Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of assembling a passive component on a die, wherein the passive component has a plurality of terminal electrodes and the die has an active surface with a plurality of bonding pads thereon, the assembling method comprising:
forming an under-bump-metallurgy (UBM) layer over the bonding pads;
forming a solder block on the UBM layer; and
bonding the terminal electrodes of the passive component to the solder block.

[c2] 2. The assembling method of claim 1, wherein the step of forming the UBM layer over the bonding pads comprises forming a re-distribution layer over the active surface coupled to the bonding pads.

[c3] 3. The assembling method of claim 1, before the step of forming the UBM layer, further comprising forming a patterned dielectric layer over the active surface of the die, wherein the patterned dielectric layer has a plurality of openings that expose the bonding pads and the UBM layer is disposed above the patterned dielectric layer.

[c4] 4. The assembling method of claim 1, wherein the step of forming the under-bump-metallurgy layer includes: forming a metallic layer over the bonding pads; and patterning the metallic layer to form the under-bump-metallurgy layer over the bonding pads.

[c5] 5. The assembling method of claim 4, wherein the step of forming the metallic layer includes one selected from the group consisting of electroplating, sputtering, and evaporation.

[c6] 6. The assembling method of claim 4, wherein the metallic layer is a composite metallic layer.

[c7] 7. The assembling method of claim 1, wherein the under-bump-metallurgy layer is a composite metallic layer.

[c8] 8. The assembling method of claim 1, wherein the step of bonding the terminal electrodes of the passive component to the solder block includes positioning the terminal electrodes in contact with the solder block and performing a reflow operation so that the solder block is melted and bonded with the terminal electrodes.

[c9] 9. A chip structure, comprising:
a die having an active surface and a back surface, wherein the active surface is implemented with a plurality of bonding pads;

an under-bump-metallurgy layer disposed over the bonding pads;
a plurality of solder blocks respectively disposed above the under-bump-metallurgy layer; and
a passive component having a plurality of terminal electrodes, which are respectively coupled to the UBM layer through the solder blocks.

[c10] 10. The chip structure of claim 9, further comprising a patterned dielectric layer over the active surface of the die, wherein the patterned dielectric layer has a plurality of openings that expose the bonding pads and the UBM layer is disposed above the patterned dielectric layer.

[c11] 11. The chip structure of claim 9, wherein the UBM layer further comprises a re-distribution layer and the re-distribution layer is electrically connected to the bonding pads.

[c12] 12. The chip structure of claim 9, wherein the under-bump-metallurgy layer is a composite metallic layer.

[c13] 13. A chip package structure, at least comprising:
a substrate having an upper surface;
a die having an active surface and a back surface, wherein the back surface of the die is in contact with the upper surface of the substrate and the active surface is

implemented with a plurality of bonding pads;
an under-bump-metallurgy layer disposed over the bonding pads;
a solder block disposed on the under-bump-metallurgy layer;
a passive component with a plurality of terminal electrodes, wherein the terminal electrodes are coupled to the under-bump-metallurgy layer through the solder block;
a plurality of conductive wires electrically connecting the die and the substrate; and
a packaging plastic enclosing the die, the passive component, and the conductive wires.

[c14] 14. The chip package structure of claim 13, wherein the UBM layer further comprises a re-distribution layer and the re-distribution layer is electrically connected to the bonding pads.

[c15] 15. The chip package structure of claim 13, wherein the under-bump-metallurgy layer is a composite metallic layer.

[c16] 16. The chip package structure of claim 13, further comprising a patterned dielectric layer disposed over the active surface of the die with a plurality of openings to expose the bond pads and the UBM layer is disposed above

the patterned dielectric layer.